Summer Research Program 2014/2015

Implementation of Polar code decoders

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Objective

The objective of this project is to optimise the HW implementation of a high speed Polar code decoder. The project will deliver a working Verilog implementation to be used for high speed simulation of polar code performance.

Description

Polar codes are a newly introduced family of error correcting codes that are capacity achieving as their length N grows to infinity [1]. The soft decoder (see Figure below) is based on a successive cancellation algorithm that has a complexity of N*log(N). A range of different solutions will be analysed to trade speed vs chip area.
Prerequisite: Experience with Verilog programming.


Fund: E03801 2415002